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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,214	02/27/2002	Laung-Terng Wang	3175-Z	7756

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,214	WANG ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *85-103* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *85-103* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL OFFICE ACTION

1. This is a FINAL Office Action in response to AMENDMENT filed 6/24/2005.

Claims 1-84 are cancelled. Claims 85-103 are new and pending.

Response to Arguments

2. Applicant's arguments with respect to claims 85-103 have been considered but are moot in view of the new grounds of rejection, as set forth in the present Office Action, below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 85-87, 89-93, 99 are rejected under 35 U.S.C. 102(e) as being anticipated by Swamy (U.S. PATENT NO: 6,686,759).

Regarding independent Claim 85, Swamy discloses an apparatus for testing embedded cores in complex, multi-core integrated circuit designs using a DFD (design-for- debug) circuitry (test circuit 40) for facilitating the testing of selected fault types in

multiple embedded cores (46-1, 46-2, 46-3 ....) each located in a corresponding circuit block (45-1, 45-2, 45-3 ...) embedded in an integrated circuit, the integrated circuit containing two or more scan cores (46-1, 46-2, 46-3 ....) each having a corresponding scan clock (TCK-1, TCK-2, TCK-3 ...) Figure 2. Each of the circuit blocks 45 is having an IC core 46, a test access port (TAP) 60, and a set of boundary-scan cells 47 connected to the core 46, in accordance with the structure shown in Figure 1, the apparatus comprising:

a) a DFD selector (multiplexer 62) having a plurality of inputs (TDO-1, TDO-2, TDO-3 ...) connected to the internal circuit blocks (45-1, 45-2, 45-3 ...), and outputting a Test Data Output (TDO) signal 66 provided by IEEE Standard 1149.1 TAP 60, for debugging scan cores (46-1, 46-2, 46-3 ....) with their fault types.

b) a scan connector, such as boundary-scan cells and a (TAP) test access port controller (not shown) contained in the multiplexing and demultiplexing hierarchical addressing scheme, Figure 5, for connecting TAP signals (Test Clock signal 50, Test Data Output signal 64, Test Data Input 68, Test Mode Select 70, and Test Reset 72) through (DEMUX) 52 and (MUX) 62 to all the test access ports 60 for controlling the operation of multiple scan chains (47-1, 47-2, 47-3 ...) coupled to scan cores (46-1, 46-2, 46-3 ....) in the integrated circuit, Figure 2.

c) a scan clock generator comprising (DEMUX) 52 and a shift register Select Register 56 for generating an ordered sequence of capture clocks (TCK-1, TCK-2, TCK-3 ...) for connecting to the scan cores (46-1, 46-2, 46-3 ....).

d) a multiplexer such as a multiplexing and demultiplexing hierarchical addressing scheme illustrated in Figure 2, for connecting the DFD selector and the scan connector to a TAP (test access port) controller in the integrated circuit.

Regarding Claim 86, Swamy discloses a scan debug mode Test Mode Select (TMS) 70, wherein the TMS mode is set to logic value 1 (HIGH) for selecting the scan cores (46-1, 46-2, 46-3 ....) during testing and set to logic value (LOW) when the scan cores are in the normal operational mode.

Regarding Claim 87, Swamy discloses wherein the scan debug mode (TMS) 70 is generated by a central DFD controller, such as an external TAP controller (not shown) contained in the multiplexing and demultiplexing hierarchical addressing scheme, Figure 2, and wherein the TAP controller is constructed in compliance with IEEE Standard 1149.1, Boundary-scan Standard which includes a test access port (TAP) comprising TDI (test data in), TDO (test data out), TCK (test clock), TMS (test mode select), and selectively TRST (test reset), Figure 2.

Regarding Claim 89, Swamy discloses wherein the DFD selector further comprising a Select Register 56 connected by n control lines 78, 79 to the select inputs of the demultiplexer 52 and multiplexer 62, respectively. The Select Register 56 is a serial shift register having n bits, each bit providing one of the n control lines 78, 79, which receives a Test Address Input (TAI) signal 74 under control of a Test Address Clock (TAC) signal 76, as shown in Figure 2.

Regarding Claim 90-92, Swamy discloses wherein the scan connector further comprises (DEMUX) 52 and (MUX) 62 to functionally connect the multiple scan chains

(47-1, 47-2, 47-3 ...) as one serial scan chain and connect the scan data input and scan data output to the TDI and the TDO, via TAP 60, respectively, wherein the multiplexers are controlled by the scan debug mode (TMS) and (TRST) signals, as shown in Figure 2.

Regarding Claim 93, Swamy discloses multiple scan chains (47-1, 47-2, 47-3 ...), which are connected in series using D, type Flip-Flops as storage lock-up elements between any multiple scan chains.

Regarding Claim 99, Swamy discloses wherein the DFD circuitry (test circuit 40) is further selected for debugging or diagnosing memory scan cores, using Test Mode Select (TMS) 70, wherein the TMS mode is set to logic value 1 (HIGH) for selecting the scan cores (46-1, 46-2, 46-3 ....) during testing and set to logic value (LOW) when the scan cores are in the normal operational mode.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 88 is rejected under 35 U.S.C. 103(a) as being unpatentable over Swamy (U.S. PATENT NO: 6,686,759).

Regarding Claim 88, Swamy substantially discloses an apparatus for testing embedded cores in complex, multi-core integrated circuit designs using a DFD (design-for- debug) circuitry (test circuit 40) for facilitating the testing of selected fault types in multiple embedded cores (46-1, 46-2, 46-3 ....) each located in a corresponding circuit block (45-1, 45-2, 45-3 ...) embedded in an integrated circuit, the integrated circuit containing two or more scan cores (46-1, 46-2, 46-3 ....) each having a corresponding scan clock (TCK-1, TCK-2, TCK-3 ...) Figure 2, r4ecited in the independent claim 85.

Swamy does not explicitly enumerate the selected fault types associated with the debugging of scan cores. It is well known in the art, that the purpose of incorporating a DFD circuitry in an integrated circuit, IC, is to detect failures under various fault conditions. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate various fault conditions, as it is well known in the art, in the apparatus of Kim, so as to evaluate the proper operation of scan cores of an integrated circuit, IC.

7. Claims 94-98 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swamy (U.S. PATENT NO: 6,686,759) in view of McLaurin et al. (U.S. PATENT NO: 6,598,192).

Regarding Claims 94-98, Swamy substantially discloses a scan clock generator (DEMUX) 52 for generating an ordered sequence of capture clocks (TCK-1, TCK-2, TCK-3 ...) for connecting to each scan clock (TCK) of each of the scan cores (46-1, 46-

2, 46-3 ....). However, Swamy does not explicitly disclose the scan clock generator further comprising "a clock phase generator and a scan clock controller".

In analogous art, McLaurin discloses a clock phase generator (programmable clock generator 220) and a scan clock controller (test controller unit 218). The programmable clock generator 220 is connected to a test clock input (input clock signal 224) from the tester 212, and provides clock signals 230 and 232 to the core 214 and peripheral logic 216. The programmable clock generator 220 manipulates the phase locked loop (PLL) output clock signals on a cycle-by-cycle basis. The test controller unit 218 provides various control signals to the core 214, peripheral logic 216, and programmable clock generator 220. When testing the IC 210, the tester 212 provides test control signals to the test controller unit 218 which put the IC 210 in a test mode.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a programmable clock generator in association with test controller unit as taught by McLaurin, in the test circuit of Swamy for providing clock signals to each core under test, since Swamy's and McLaurin's test circuits are both in compliance with the IEEE Standard 1149.1, Boundary Scan, TAP interface, and as such, the interface design implementation does not require additional hardware. Furthermore, a person skilled in the art would have been motivated to do so, since the clock generator includes a phase locked loop (PLL), which provide a desired waveform to the IC for testing purposes, so that when used in conjunction with a tester, the IC can be scan tested at-speed using slower and less expensive testing equipment, see Abstract.

8. Claims 100-103 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. Patent No. 6,122,762) in view of Swamy (U.S. PATENT NO: 6,686,759).

Regarding independent Claim 100, Kim substantially discloses a method for diagnosing scan cores (310), having an embedded DFD (design-for-debug) circuitry in a memory interface device (40), the DFD circuitry comprising a debug controller 400 and a JTAG TAP circuit 100, Figure 3, which is a state diagram of the TAP controller 10 of Figure 1. The TAP controller 10, driven by the TCK input, responds to the TMS input as shown, the method comprising the steps of:

(a) Issuing a DBG SCAN command (DRAM_debug) generated as a result of the test/debug instruction form register 210 to control the debug controller 400 and a JTAG TAP circuit 100 in the scan cores.

(b) Issuing a SELECT command (SELECT_DR_SCAN) for shifting in selected scan cores for diagnosing the scan cores by the debug controller 400 and a JTAG TAP circuit 100.

(c) Issuing a first SHIFT command (SHIFT_DR) for shifting in a predetermined scans pattern (TDI) to scan cells within selected scan chains for diagnosis.

(d) Issuing one or more CAPTURE (CAPTURE_DR) commands for capturing output responses into the scan cells.

(e) Issuing a second SHIFT command (SHIFT_IR) for shifting a new predetermined scan pattern (TDI) into and out of the scan cells within the selected scan chains (boundary-scan chain 332).

(f) Repeating steps of (d)-(e) by capturing and shifting the data out of the (boundary-scan chain 332) until scan diagnosis is done.

(g) Issuing a STOP command (PAUSE_DR) for generating a stop control signal to stop the scan operation.

However, Kim fails to disclose, "two or more scan cores each having a scan clock in an integrated circuit".

In analogous art, Swamy discloses a method for testing multiple embedded cores (46-1, 46-2, 46-3 ....) each located in a corresponding circuit block (45-1, 45-2, 45-3 ...) embedded in an integrated circuit, the integrated circuit containing two or more scan cores (46-1, 46-2, 46-3 ....) each having a corresponding scan clock (TCK-1, TCK-2, TCK-3 ...) Figure 2. Each of the circuit blocks 45 is having an IC core 46, a test access port (TAP) 60, and a set of boundary-scan cells 47 connected to the core 46, in accordance with the structure shown in Figure 1.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the memory interface device of Kim, so as to incorporate multiple embedded cores with their corresponding boundary-scan chains and scan clocks, in compliance with the IEEE Standard 1149.1, Boundary Scan, TAP interface, as taught by Swamy, for the purpose of debugging faults in multiple scan cores, since Kim's and Swamy's test circuits are both in compliance with the IEEE Standard 1149.1, Boundary Scan, TAP interface, and as such, the interface design implementation does not require additional hardware.

Regarding Claim 101, Kim discloses providing a central DFD controller (400) for accepting the commands and generating the scan debug mode (DRAM_debug) and the stop control signal (PAUSE_DR) to control the debug controller 400 and a JTAG TAP circuit 100.

The DFD controller 400 interfaces with the DFD circuitry and a JTAG TAP circuit 100 in the integrated circuit 40, and wherein the TAP controller 100 is constructed according to a selected Boundary-scan Standard, Figure 4.

Regarding Claim 102, Kim substantially discloses the claimed invention as applied to independent claim 100, above. However, the combined reference of Kim and Swamy does not explicitly enumerate the different faults for associated with the scan cores. It is well known in the art, that the purpose of incorporating a DFD circuitry in an integrated circuit, IC, is to diagnose failures under various fault conditions. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate various fault conditions in the combined reference of Kim and Swamy as it is well known in the art, so as to evaluate the proper operation of scan cores of an integrated circuit, IC.

Regarding Claim 103, Kim discloses the commands are further used in a DFD circuitry in a memory interface device (40) comprising a debug controller 400 and a JTAG TAP circuit 100, for diagnosing scan cores (310), Figure 4.

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2133

By: _____

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Date: 23 September 2005
Office Action: Final Rejection

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